Investor Presentation

December 2019
NASDAQ: MOSY

Safe Harbor Statement

This presentation may contain forward-looking statements about MoSys, Inc. (the Company) for purposes of Section 27A of the Securities Act of 1933, as amended, and Section 21E of the Securities Exchange act of 1934, as amended, including, without limitation, benefits and performance expected from use of its embedded memory and interface technologies and integrated circuit (IC) products, improving operational efficiencies, the timing of product development and shipments of the Company's IC products, anticipated benefits and performance expected from the Company's IC products, growth in the size of the market addressed by the Company's business, future markets and future business prospects. Forward-looking statements are based on certain assumptions and expectations of future events that are subject to risks and uncertainties. Actual results and trends may differ materially from historical results or those projected in any such forward-looking statements depending on a variety of factors. These factors include, but are not limited to the following:

- a lack of working capital to aggressively fund product development and growth;
- achieving additional design wins for our IC products through the acceptance of our IC architecture and interface protocols by potential customers and their suppliers;
- the timing of customer orders and product shipments;
- customer concentration;
- lengthy sales cycle;
- our ability to enhance our existing proprietary technologies and develop new technologies;
- achieving necessary acceptance of our IC products by equipment suppliers to the cloud networking, data center, security and other systems markets;
- difficulties and delays in the development, production, testing and marketing of our IC products;
- reliance as a fabless semiconductor manufacturer on our manufacturing partners to assist successfully with the fabrication of our ICs;
- availability of quantities of ICs supplied by our manufacturing partners at a competitive cost;
- ability to make our new software acceleration and IP products commercially available and achieve customer acceptance of these new proprietary technologies;
- level of intellectual property protection provided by our patents, the expenses and other consequences of litigation, including intellectual property infringement litigation, to which we may be or may become a party from time to time;
- vigor and growth of markets for cloud networking, data center, security and other systems served by our licensees and customers; and

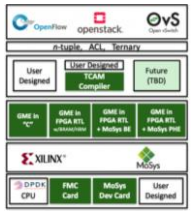
other risks identified in MoSys' most recent reports on form 10-K and form 10-Q filed with the Securities and Exchange Commission, as well as other reports that MoSys files from time to time with the Securities and Exchange Commission. MoSys undertakes no obligation to update publicly any forward-looking statement for any reason, except as required by law, even as new information becomes available or other events occur in the future.

About MoSys

- **Silicon Valley fabless semiconductor company providing Silicon devices and software/firmware IP**

- **Silicon Accelerator Engine Intelligent Memory ICs**
  - High-speed serial attached memories for FPGA applications
    - Patented Serial high-speed Interface (signal connections)
    - Intelligent In-Memory functions

- ***New*…Software Solution Function Platforms**
  - High Value, High Level Application Functions
  - Software Products & FPGA Firmware IP (Intellectual Property)
  - Portable Functions across range of Performance-Scaled Hardware



- **High-Speed PHY (Serial Signal) IC products**
  - Signal conditioning, Gearbox, Retimers

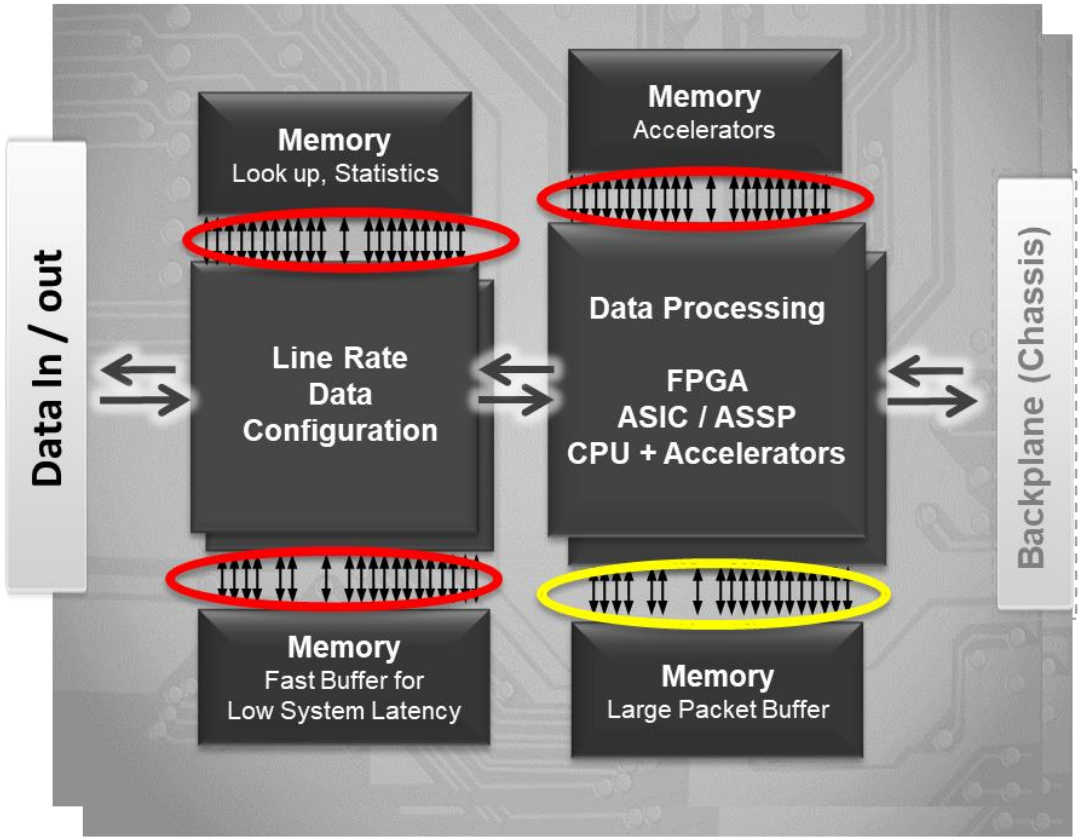
- **Products are Market/Customer performance validated**
  - Palo Alto Networks, Nokia, Fujitsu, etc.

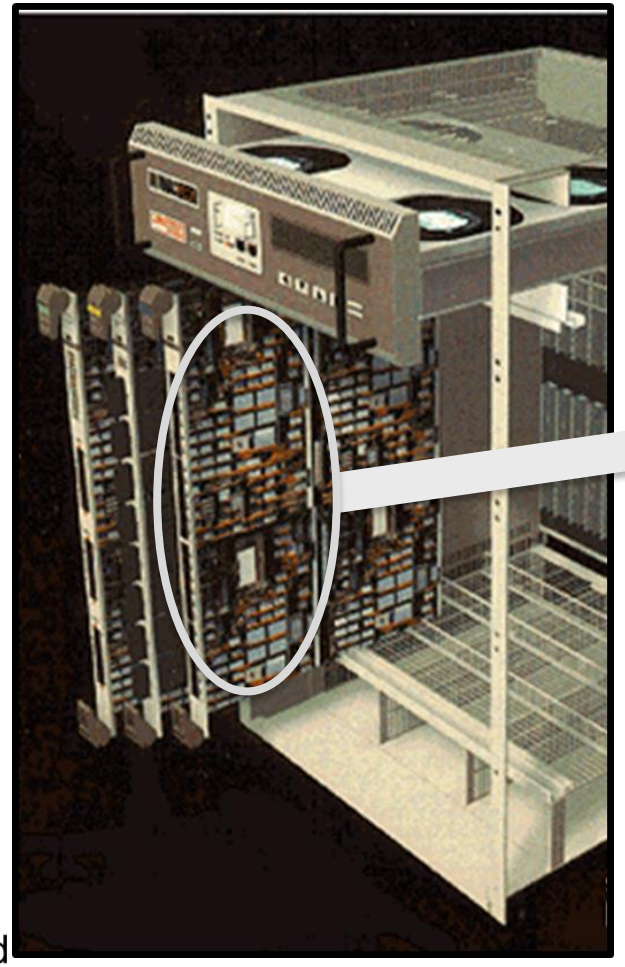
NASDAQ: MOSY
ISO 9001:2008 Certified
HQ: San Jose, CA
~115 Patents & Pending

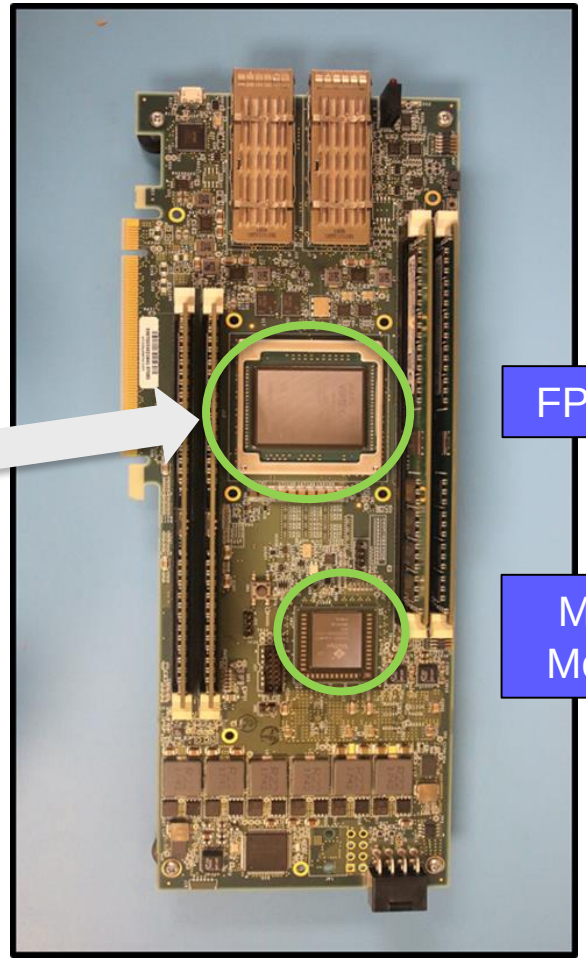
Acceleration options Not available in any other competing product

Silicon Accelerator Engine Memory ICs

Packet / Data Processing Cards







Data Processing Card Functions:
Router, Switch, Security, Monitor/Test, Video, Server Offload

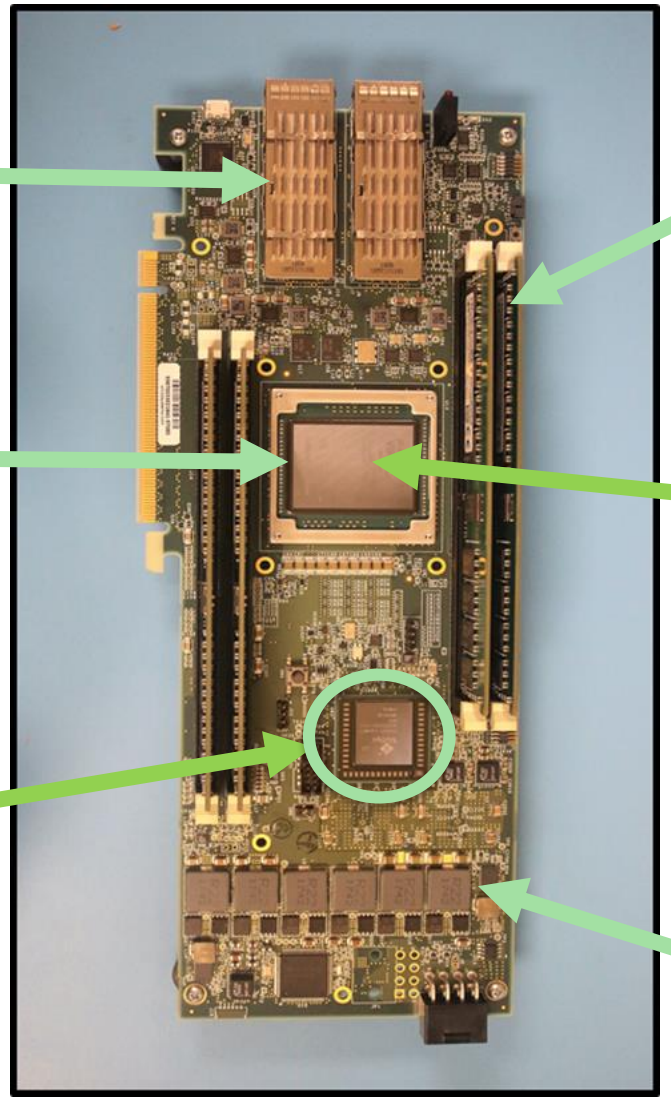
Typical High-Volume Accelerator Cards

INPUT & OUTPUT

FPGA

(Field Programmable Gate Array)

MoSys High-Speed Memory Serial attached to the FPGA



DRAM

***New* - MoSys Software Platform Embedded in FPGA**

POWER CONTROL

FPGA is a $5B market for Intel (Altera) & Xilinx

MoSys Accelerates FPGA Application Performance

Intel/Xilinx FPGA

Application RTL

High-level function

Low/High-level function

Basic Function

RTL memory & Input/out I/F

MoSys attaches to high-speed FPGAs

- Intel
- Xilinx

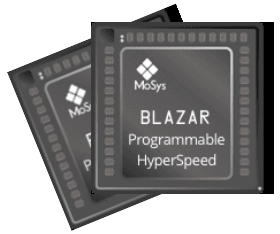
FPGA is reprogrammable!

- Logic is defined with FPGA RTL software
- Defines:
  - Logical flow of information & Control
  - Function execution
  - Data manipulation
  - Input/Output control
- **Most functions need external Memory**

MoSys High-Speed Memory

DRAM Memory

Inputs/Outputs

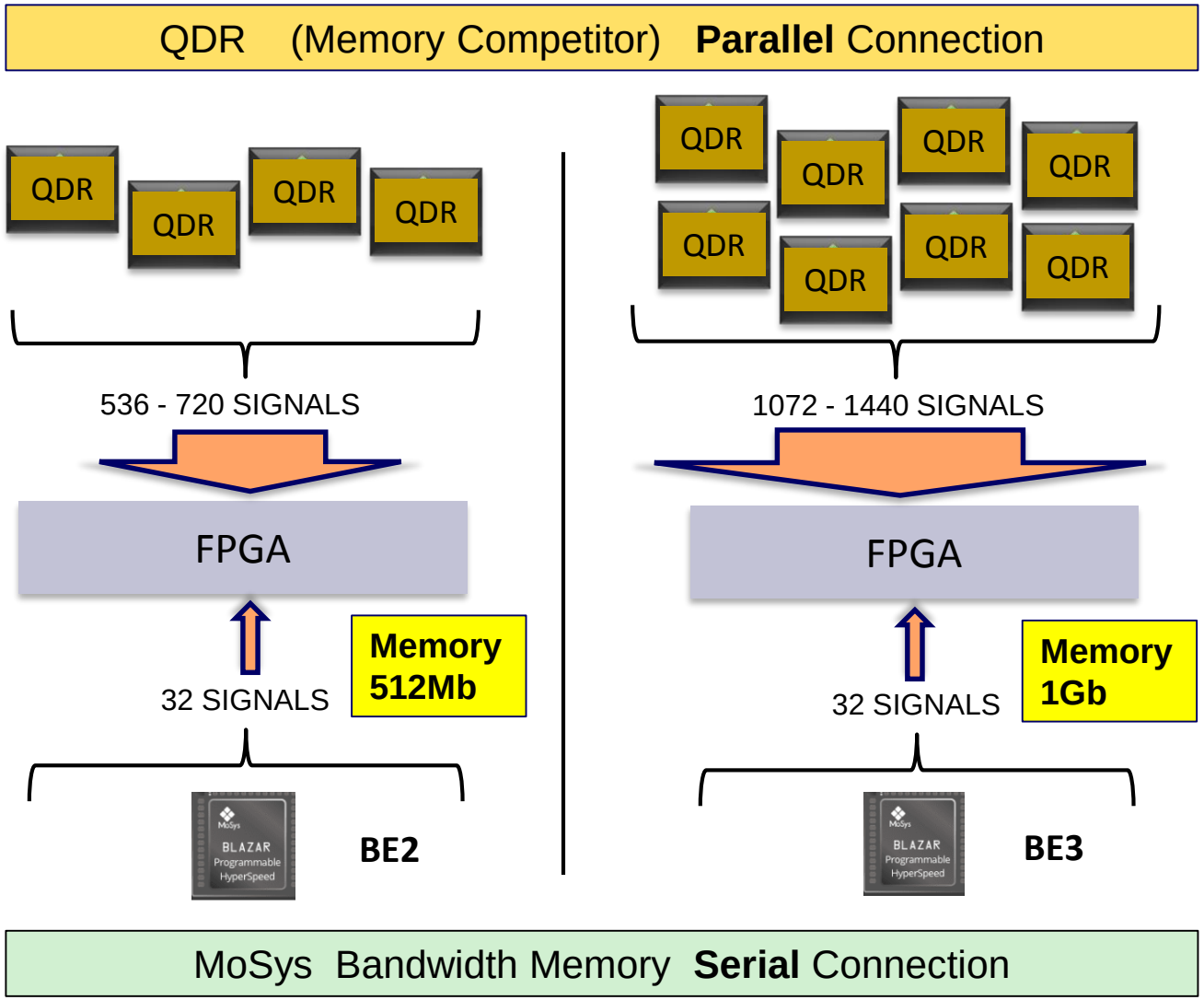


BLAZAR Accelerator Engine IC Products (AE)

- Bandwidth Engine Silicon ICs
  - High-Speed serial attached memories
  - Large memory sizes
    - 512Mb
    - 1Gb
  - Differentiated by In-Memory
    - Intelligent functions
- Programmable HyperSpeed Engine IC
  - Bandwidth Engine with 32 computer cores

Saves Space/Cost

Serial vs Parallel Memories



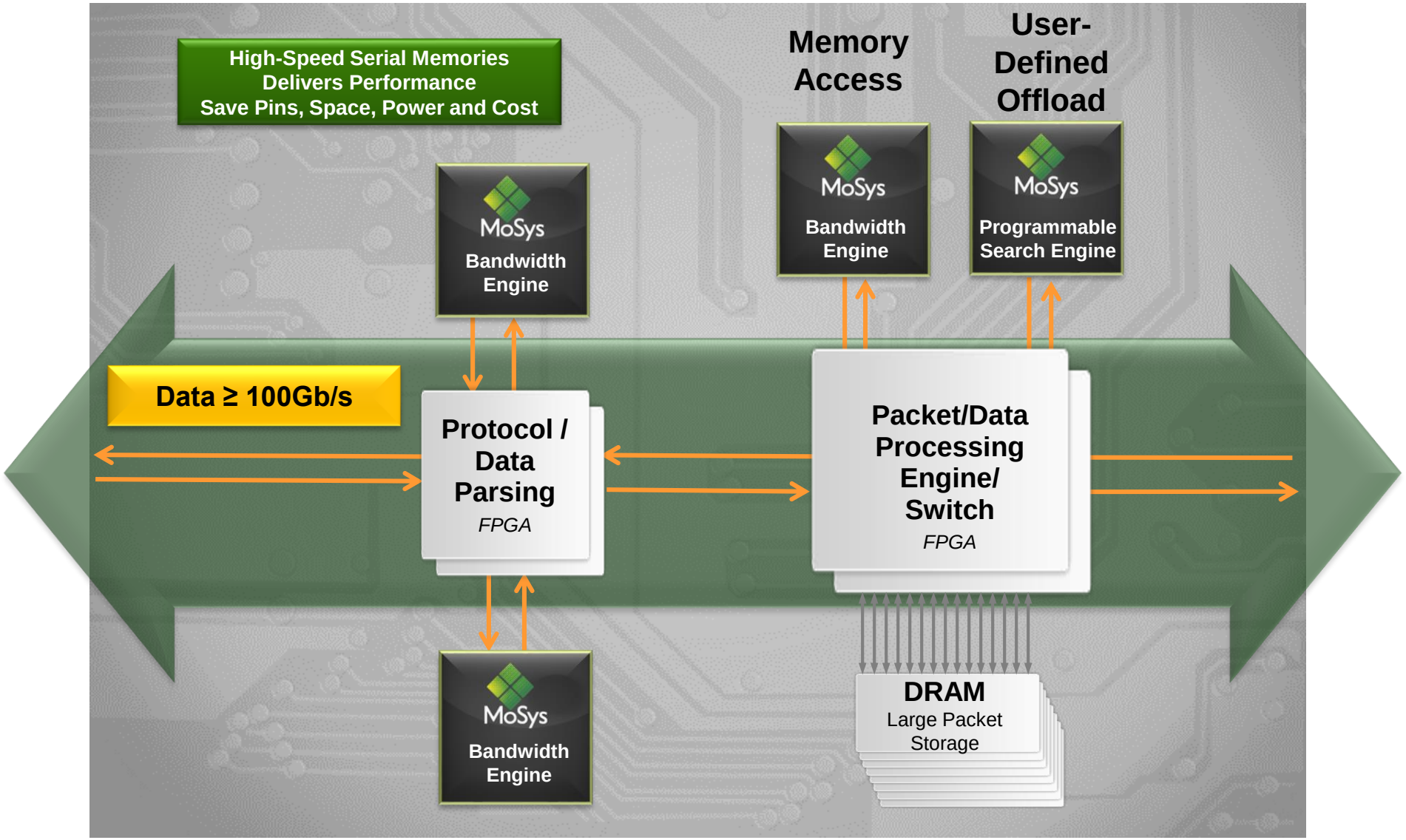
Space & Cost Considerations

Performance Balance of Memory vs Space

- Space
  - BE2 = 4 QDR … 512Mb
  - BE3 = 8 QDR … 1Gb
- Part Cost
  - 1-BE2 for 512Mb memory ~ 2x cost of one QDR
    - 4x Memory
  - 1-BE3 for 1Gb memory ~ 2.5x cost of one QDR
    - 8x Memory
- Design time
  - Signal routing time and layout
  - Told it saved 6-9 months
- Signal Integrity
  - 536-1440 clean signals
    - External components
  - MoSys on board signal tuning
    - No external components
- Power
  - ~ Half
- Bandwidth
  - Random data access is equivalent
  - For certain applications, much faster

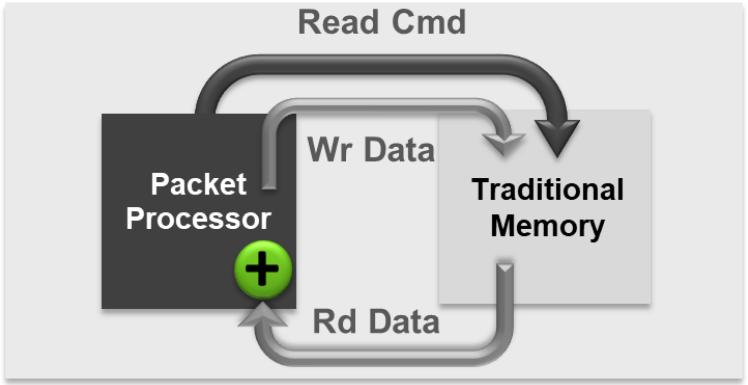
MoSys Intelligent Serial Memory

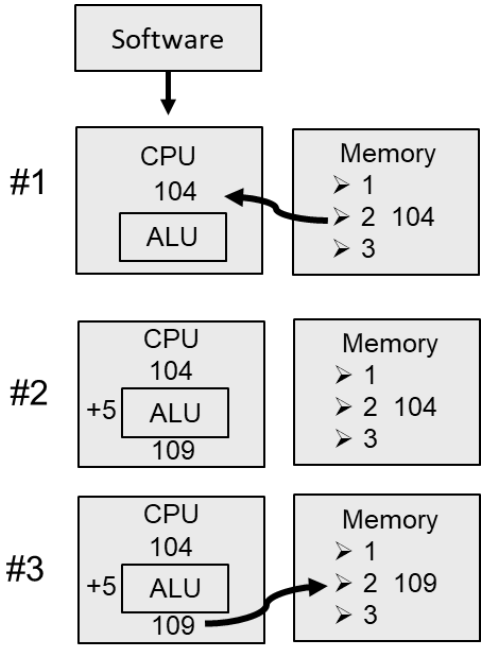
For Networking to Testers to Video to IOT… when speed is key!



Acceleration with MoSys In-Memory Execution

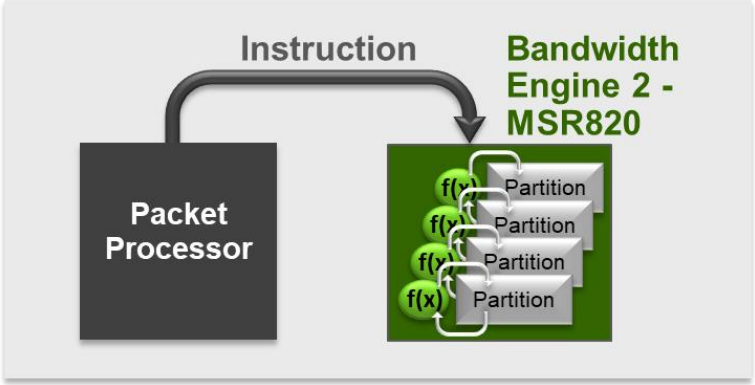
CURRENT

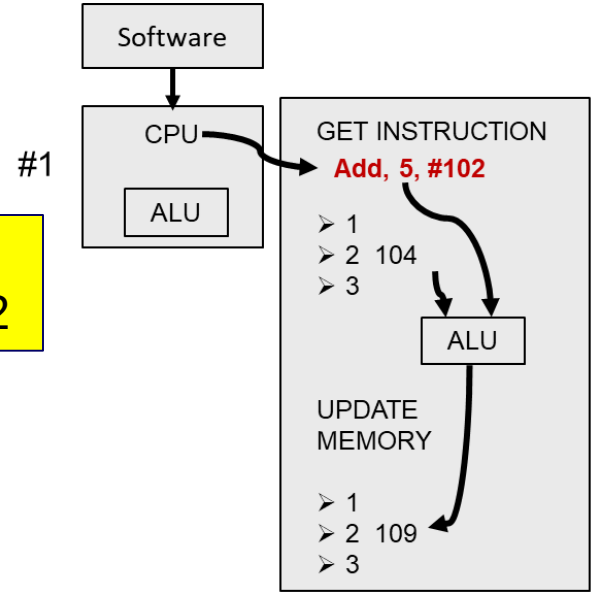




FUNCTION:
ADD, 5 to Loc #2

MoSys IN-MEMORY





MoSys In-Memory Functions

Standard in all MoSys ICs

- BURST
  - Multiple Sequential READS
  - Multiple Sequential WRITES
  - Function types ~12
- RMW (Read-Modify-Writes)
  - ADD, SUB, INC, Compare, etc.
  - Functions ~17

Accelerating FPGA Applications with Speed & Intelligence

Application RTL

High level function

Low/High-level functions

Basic Function

RTL memory I/F

Increasing Acceleration

Programmable HyperSpeed AE IC
- Intelligent In-Memory
  - Functions Burst/RMW
  - User Programmable Functions
  - MoSys supplied functions (future)

Bandwidth AE IC
- Intelligent In-Memory
  - Functions Burst/RMW

Bandwidth AE IC
- **Just a Memory!**

BE 2
BE 3
512Mb/1Gb

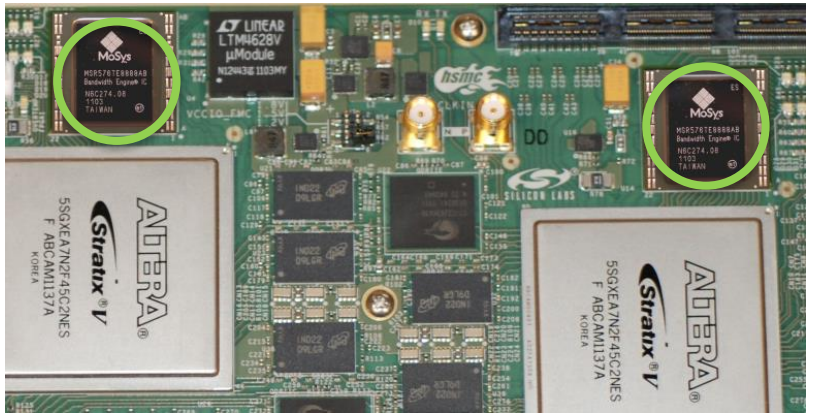
BE2
BE3

Embedded
Burst
RMW

PHE
- BE3 based with Embedded Burst & RMW
- 32 RISC Cores
- Embedded Functions
  - User defined
- MoSys define
  - Functions
  - Algorithms

MoSys Value Proposition
Speed-Signals-Space-Cost

Bandwidth Engine relieves key system constraints



Attribute	Competition QDR SRAM/ RLDRAM	MoSys Bandwidth Engine
Speed	80-800Gb/s	
Number of Chips	4 - 8	1
Pin Count (Signals)	526-1440	32
Power (W)	14 - 28	8 - 16
Markets - Broad	Any High-Speed FPGA with Memories Attached	

4-8x more Memory

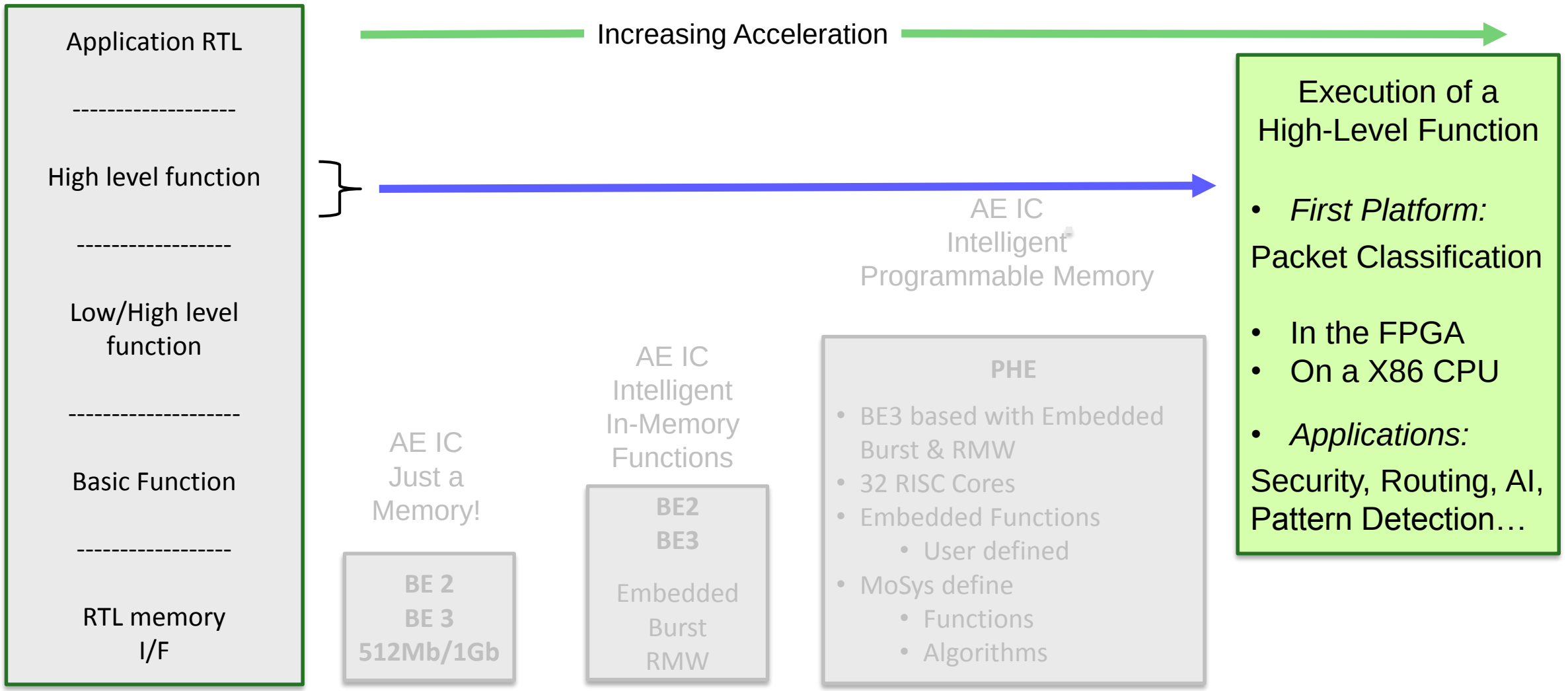
85-95% less Pins

~ 50% less power

Source: Company Management

New…Virtual Accelerator Software Platforms

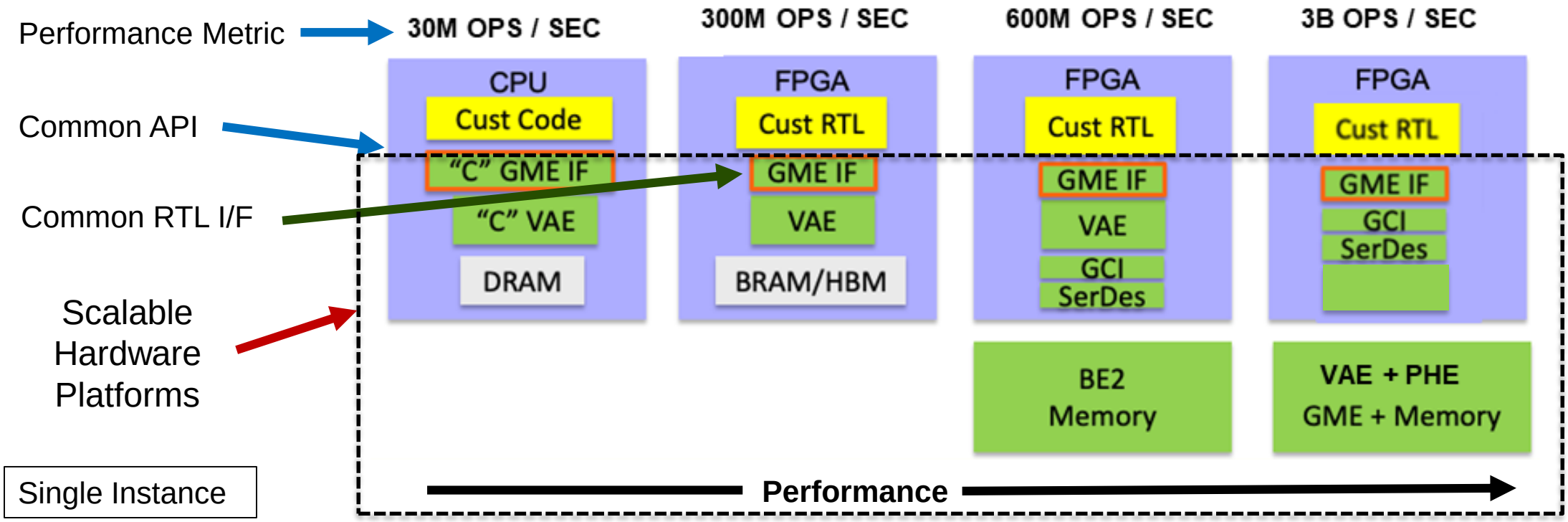
Capturing more dollar value of the solution!



Virtual Accelerator Engine Platform
Software Portability – Scalable Agnostic Hardware

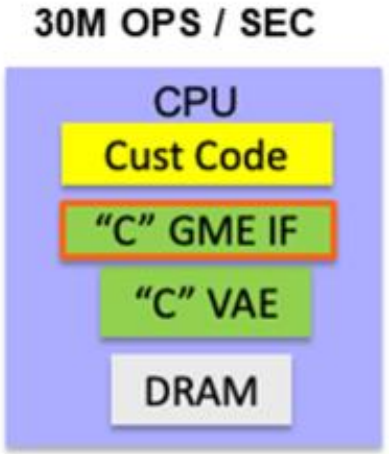
- *Software Goal*: Software Portability
  - Common API
    - Application Programming Interface
      - Set of Instructions

- *Hardware Goal*: Hardware Agnostic
- Common RTL Interface
  - FPGA Code
    - Performance Scalable Hardware Solutions



VAE – Software and FPGA IP

SOFTWARE ONLY



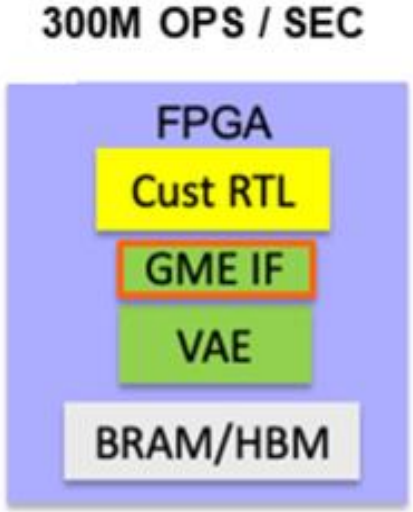
Characteristics

- Runs on any X86 system
- Software Only

Implementation

- Use S/W API
- Existing systems Acceleration

FPGA RTL – IP in the FPGA



Characteristics

- *10x over Software Only*
- Does not require MoSys AE ICs

Implementation

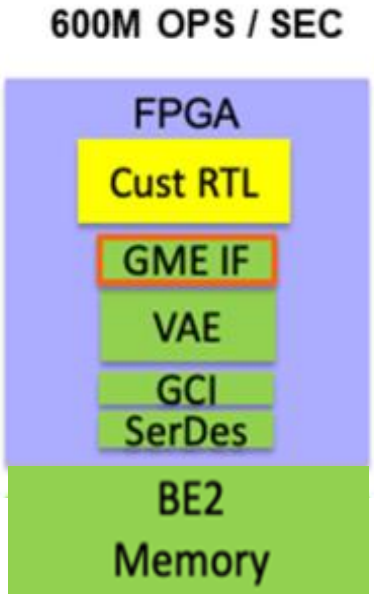
- Embedded IN THE FPGA
- Uses API and RTL
- Existing systems Acceleration

KEY POINTS

- MoSys *NOW* offering Software and IP products - *NEW* Revenue Stream
- Does not require MoSys Silicon Accelerator Engines ICs
  - BE2/3 or PHE
- Works with Existing Hardware designs
- Short time to Revenue --- Design License (Up Front) – Use License per system

VAE – FPGA with Accelerator Engine ICs

FPGA with Bandwidth Engine (BE)



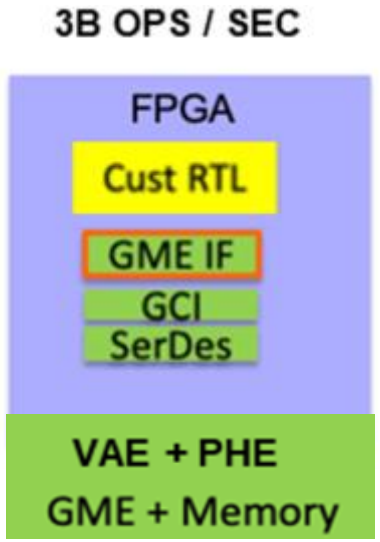
Characteristics

- *2X the performance of FPGA only*
- GME located in FPGA
- Uses AE High Speed Memory

Implementation

- Requires hardware design

FPGA with Programmable HyperSpeed Engine



Characteristics

- *5X the performance of BE*
- *100X the Software only*
- Uses PHE – Memory/32 CPUs
  - GME located in PHE
- *Extreme Acceleration*

Implementation

- Requires hardware design

KEY POINTS

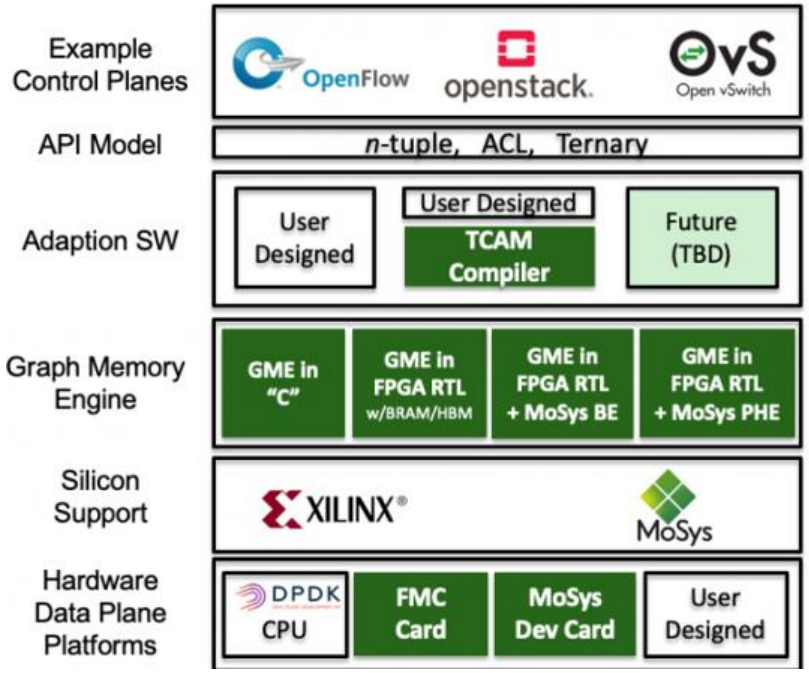
- Much Higher Performance WITH Bandwidth Engine IC
- “HyperSpeed” Acceleration with Programable HyperSpeed Engine IC
- Short time to Revenue --- Design License (Up Front)
- Delayed Revenue --- Use License per system

First …Packet Classification Platform
Software Portability – Hardware Agnostic

Applications: Security, Routing, AI, Pattern Detection…

- *Software Goal*: Software Portability
  - Designers determine Software performance required
- *Hardware Goal*: Scaled performance hardware solutions
  - Hardware environment is selected

"SOFTWARE DEFINED/HARDWARE ACCELERATED"



MoSys Software & Firmware IP

- ***Potential New Revenue Streams***
- ***New Markets and Applications***

- *NOT dependent on using MoSys AE ICs*
- *Legacy Systems -- No H/W redesigns required*
- *New BE H/W designs --High Acceleration*

Short time to revenue

- License – Upon engagement
- Royalty Use – Implementation
  - Add to Existing systems
    - Reprogram the FPGA
    - Quick Time to Market
- Current customer engagements

GME = Graph Memory Engine will Support new Future Platform!

Accelerator Engine Product Lines

IC Accelerator Engines (AE)

Target Performance Based---
Point Products

Bandwidth Engine

BE2 Family based with 512 Mb memory

BE3 Family based with 1Gb memory

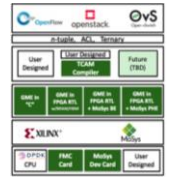
In-Memory AccelertionFunctions
- Burst (12+)
- RMW with ALU (17+)

Programmable HyperSpeed Engine

PHE
- BE3 with 1Gb memory
- 32 CPU cores
- In-Memory Functions
  Burst/RMW
- Use defined functions
- Future MoSys embedded functions

Virtual Accelerator Engines (VAE)

Software Portability Based---
Solution Products



Virtual Accelerator Engines- GME
API Software Based

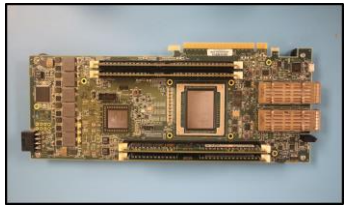
***First* - Packet Classification Platform**

*Common API
- Transportable software
- Family of products

*Common RTL
- Scalable performance
- Selectable Hardware

Product/Application (*Stacking*) can be
- Software only
- RTL (FPGA) *(New & Existing designs)*
- RTL(FPGA) with BE2 or BE3
- RTL (FPGA) with PHE

Dev/ Ref boards



- Cheetah Xilinx PCIe
- FMC Dev Card

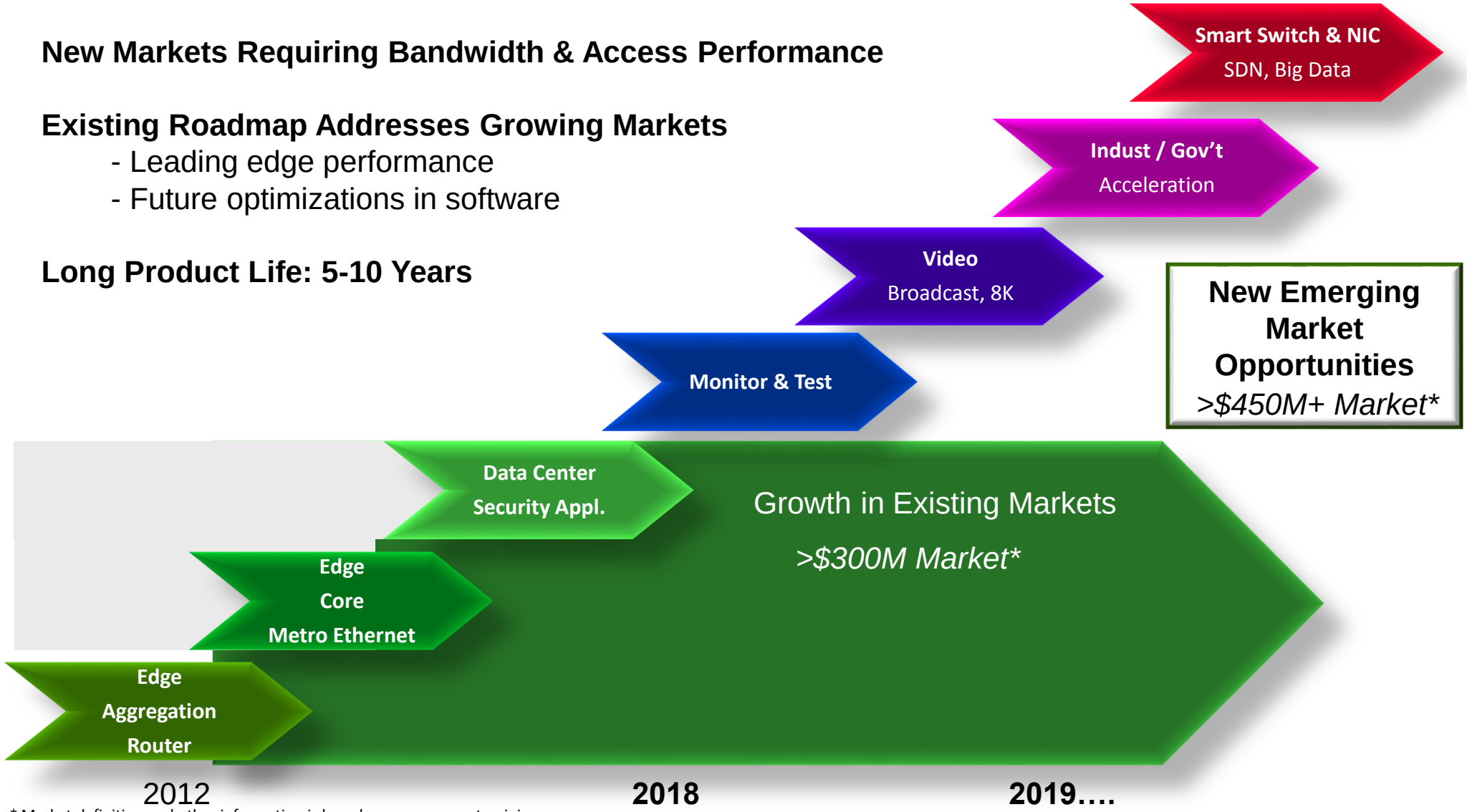
Expanding Market Opportunities

New Markets Requiring Bandwidth & Access Performance

Existing Roadmap Addresses Growing Markets

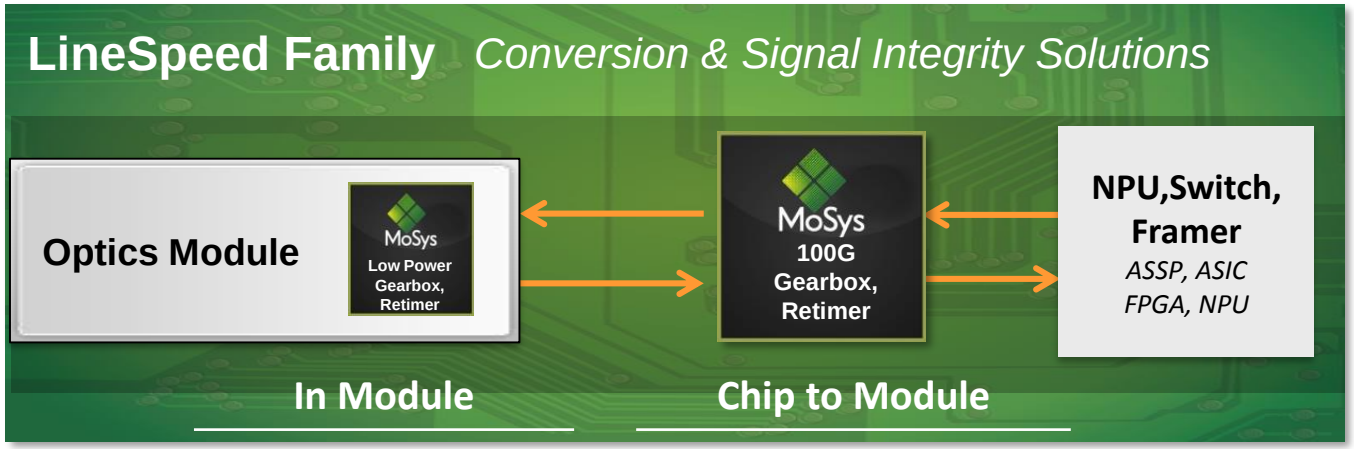
- Leading edge performance
- Future optimizations in software

Long Product Life: 5-10 Years



* Market definition and other information is based on management opinion.

LineSpeed™ 100G PHY Products



LineSpeed PHY Family	In Module	Chip to Module
	MSH321 (S) 100G MLG Gearbox	MSH320 100G Gearbox w/FEC
	MSH221 (S,F) 100G Octal Retimer w FEC	MSH322 MLG Gearbox
		MSH225 10 Lane Full Duplex Retimer
		MSH222 100G FD Quad Retimer w/FEC

- Industry-standard interfaces
- Flexible Gearbox, Retimer and FEC functions
- Strong signal Integrity
- Low-power options

Investment Highlights

- **History of impacting markets with unique products/IP**
- **Product portfolio has major customer validation**
- **Highly-differentiated products with attractive gross margins**
  - High ASP and high-margin products
  - Limited competition
  - Proprietary products build long-term partnerships
- **Sales & Marketing focused on expansion**
  - Sales Channels
  - Into Large New Markets
  - Into New Applications
- **Best of both worlds… Hardware and '*now*' Software**
  - Silicon IC based Accelerator Engine for Broad Markets…High margin
  - Software Platforms --- Potential New Revenue Stream of Software & Firmware IP
    – Target for specific solutions high value performance solutions
    – Does not require MoSys ICs…Higher performance with MoSys ICs
    – Shorter time to Revenue…Target Model - License Design/Use Royalty

Accelerator Products: Fast, Intelligent Solutions

Experienced Management Team

Dan Lewis CEO	GMS, XICOR, IDT, zilog, intel
Jim Sullivan CF0	8x8, Apptera, pwc
Gus Lignos VP Sales	NVIDIA, tensilica, IDT, avangate IS NOW 2checkout, NEC
Michael Miller CTO	IDT, AMD
Sinan Doluca VP Engineering & Operations	EXCLARA, PMC PMC-SIERRA, QED Quantum Effect Devices, CHIPS CHIPS AND TECHNOLOGIES, INC., AMD

Summary Income Statements

$ in millions, except EPS

Non-GAAP*	2018	1Q 19	2Q 19	3Q 19	YTD2019
Total Revenue	$ 16.6	$ 3.5	$ 3.1	$ 1.2	$ 7.8
Product	$ 15.1	3.4	2.8	1.0	7.2
Royalty/other	1.5	0.1	0.3	0.2	.6
Product GM %	*58%*	60%	59%	61%	60%
Total GM %	*62%*	62%	60%	66%	62%
R&D	*3.7*	1.2	0.9	1.1	3.2
SG&A	3.7	0.9	0.9	1.0	2.8
Total Op Ex	7.4	2.1	1.8	2.1	6.0
Op Income (loss)	2.8	-	-	(1.3)	(1.2)
Net Income (loss)	$ 2.2	$ -	$ -	$ (1.3)	$ (1.3)
Adjusted EBITDA**	$ 3.4	$ 0.1	$ 0.1	$(1.2)	$(1.0)
EPS (basic)	$ 0.15	$ -	$ -	$(0.60)	$(0.59)

Key Initiatives:

- **Establish Sales & Operational Scale**
- **Achieve/Maintain Profitability**
- **Reduce Cash Burn**
- **Improve Cash Position**

* Non-GAAP: Excludes stock-based compensation, amortization of intangibles and restructuring/impairment charges. See reconciliation of GAAP to non-GAAP results on slide 22.

** Adjusted EBITDA defined as GAAP net income (loss) before interest expense, income tax provision, depreciation and amortization, as well as stock-based compensation, intangible asset amortization and restructuring/impairment charges. See reconciliation of GAAP to non-GAAP financial information on slide 21.

Balance Sheet

	Q3 - September 30, 2019 *(in millions)* Actual
Cash	$6.8
Total Assets	$10.1
Deferred Revenue	$0.1
Convertible Notes* (Long-Term)	$2.9
Total Liabilities	$4.6
Stockholders' Equity	$5.5
Total Shares Outstanding	2.2

* Key terms: i) Interest rate 8% (PIK at company's option), ii) Convert price - $11.40 per share, iii) $2.9M due in full in August 2023 and iv) no covenants

Investment Highlights

- **History of impacting markets with unique products/IP**
- **Product portfolio has major customer validation**
- **Highly-differentiated products with attractive gross margins**
  - High ASP and high-margin products
  - Limited competition
  - Proprietary products build long-term partnerships
- **Sales & Marketing focused on expansion**
  - Sales Channels
  - Into Large New Markets
  - Into New Applications
- **Best of both worlds… Hardware and '*now*' Software**
  - Silicon IC based Accelerator Engine for Broad Markets…High margin
  - Software Platforms --- Potential New Revenue Stream of Software & Firmware IP
    – Target for specific solutions high value performance solutions
    – Does not require MoSys ICs…Higher performance with MoSys ICs
    – Shorter time to Revenue…Target Model - License Design/Use Royalty

Accelerator Products: Fast, Intelligent Solutions

Thank You

Dan Lewis
President & CEO
408-418-7581
dlewis@mosys.com

Jim Sullivan
Chief Financial Officer
408-418-7582
jsullivan@mosys.com

Reconciliation of GAAP and Non-GAAP Financial Information

$ in 000s

	2018	1Q 19	2Q 19	3Q 19	YTD 2019
GAAP net income (loss)	($ 11,410)	$ 10	($ 103)	($ 1,801)	($ 1,894)
Stock-based compensation expense	675	(4)	119	84	199
Restructuring & impairment charges	12,856	-	-	420	420
Amortization of intangibles	112	-	-	-	-
Non-GAAP net income (loss)	2,233	6	16	(1,297)	(1,275)
EBITDA adjustments:					
Depreciation	598	72	39	37	148
Interest expense	551	54	56	54	164
Provision (benefit) for income taxes	14	-	-	-	-
Adjusted EBITDA	$ 3,396	$ 132	$ 111	($ 1,206)	($ 963)